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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,389	11/08/2001	Matthew Becker	SMQ-143/P6594	4465

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/010,389	BECKER ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 18 objected to because of the following informalities: In line 4, please change the limitation "a advancing mechanism" to "an advancing mechanism". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Panwar et al., US Patent 6,098,165 (herein referred to as Panwar).

4. Referring to claim 1, Panwar has taught a method for calculating the number of valid instructions within a microprocessor (Figure 7, element 710 stores the calculated number of valid instructions within the microprocessor.) comprising:

a. advancing instructions along a microprocessor pipeline (Figures 2 and 6, element 604, column 3, lines 15-37, column 4, lines 53-61); and

b. edge detecting valid instructions within the microprocessor pipeline (The system of Panwar is clocked. At each active clock cycle edge valid instructions are detected and marked as such in element 710 of Figure 7.).

5. Referring to claim 2, Panwar has taught a method for calculating the number of valid instructions within a microprocessor (Figure 7, element 710 stores the calculated number of valid instructions within the microprocessor.) comprising:

a. fetching a bundle of instructions (Figures 3, 5, and 9, element 203 is a bundle of fetched instructions.); and

b. edge detecting valid instructions within the bundle (The system of Panwar is clocked. At each active clock cycle edge valid instructions are detected and marked as such in element 710 of Figure 7.).

6. Referring to claim 3, Panwar has taught a method according to claim 2, as described above, and further comprising shifting at least one instruction within the bundle (Figures 5-9, Each instruction in the bundle is shifted to a sub-bundle.).

7. Referring to claim 4, Panwar has taught a method according to claim 3, as described above, and further comprising shifting at least one instruction based at least in part on the number of valid instructions in the bundle (Figures 5-9, The shifting of the instructions in the bundle is based on the number of valid instructions, as indicated by element 710.).

8. Referring to claim 5, Panwar has taught a method according to claim 3, as described above, and further comprising compressing the bundle of instructions (Figures 5-9, The instruction bundle is compressed into several smaller sub-bundles.).

9. Referring to claim 6, Panwar has taught a method according to claim 3, as described above, and further comprising compressing the bundle of instructions for a monotonic instruction bundle (Figure 5, element 500A is a monotomic instruction sub-bundle since all of the valid instructions are at the top of the sub-bundle.).

10. Referring to claim 7, Panwar has taught a method according to claim 3, as described above, and further comprising compressing the bundle of instructions based at least in part on the number of valid instructions in the bundle (Figure 5, Bundle 203 is compressed to element 500A with 3 instructions. This compression is based on the fact that the first three of the instructions in the bundle are valid.).

11. Referring to claim 8, Panwar has taught a method, comprising:

a. fetching a bundle of instructions having a complex instruction (Figure 2, element 202, Figures 3 and 5, element 203, element D);

b. shifting at least one instruction occurring after the complex instruction (Figure 5, element 500C, elements E, F, G, and H are shifted to sub-bundle 500C, after the complex instruction, element D in sub-bundle 500B.); and

c. edge detecting the number of valid instructions occurring after the complex instruction (The system of Panwar is clocked. At each active clock cycle edge valid instructions are detected and marked as such in element 710 of Figure 7.).

12. Referring to claim 9, Panwar has taught a method according to claim 8, as described above, and further comprising bundling instructions occurring prior to the complex instruction (Figure 5, element 500A, Instructions A, B, and C are bundled in element 500A, prior to complex instruction D in sub-bundle 500B.).

13. Referring to claim 10, Panwar has taught a method according to claim 8, as described above, and further comprising executing instructions occurring before the complex instruction (Figure 2, Figure 6, element 604).

14. Referring to claim 11, Panwar has taught a method according to claim 8, as described above, and further comprising bundling instructions occurring after the complex instruction (Figure 5, element 500C, Instructions E, F, G, and H, which are after complex instruction D, are bundled in sub-bundle 500C.).

15. Referring to claim 12, Panwar has taught a method according to claim 8, as described above, and wherein the step of shifting the instructions comprises compressing the instructions occurring after the complex instruction (Figure 5, element 500C, elements E, F, G, and H are compressed into the smaller sub-bundle 500C, after the complex instruction, element D in sub-bundle 500B.).

16. Referring to claim 13, Panwar has taught a method according to claim 8, as described above, and wherein the step of shifting the instructions comprises compressing the instructions occurring after the complex instruction for a monotonic instruction bundle set (Figure 5, element 500C).

17. Referring to claim 14, Panwar has taught a method according to claim 8, as described above, and further comprising executing instructions occurring prior to the complex instruction during a first clock cycle (column 10, lines 4-22).

18. Referring to claim 15, Panwar has taught a method according to claim 14, as described above, and further comprising executing the complex instruction during a second clock cycle (column 10, lines 4-22).

19. Referring to claim 16, Panwar has taught a method according to claim 15, as described above, and wherein the step of shifting the instructions within an instruction bundle occurs while at least one of the instructions occurring prior to the complex instruction are executed and the

complex instruction is executed (Figure 5, element 500C, elements E, F, G, and H are shifted to sub-bundle 500C while the complex instruction, D, and the prior instructions, A, B, and C, are executed.).

20. Referring to claim 17, Panwar has taught a method, comprising:

a. fetching a bundle of instructions having a complex instruction (Figure 2, element 202, Figures 3 and 5, element 203, element D);

b. executing during a first clock cycle valid instructions occurring prior to the complex instruction (column 10, lines 4-22, Instructions A, B, and C);

c. executing the complex instruction during a second clock cycle (column 10, lines 4-22, Instruction D);

d. shifting instructions within the bundle occurring after the complex instruction during at least one of the first clock cycle and the second clock cycle (column 10, lines 4-22, During the first and second clock cycles instructions E, F, G, and H are shifted to the third sub-block, element 500C, so that the complex instruction is allowed to expand and execute the second clock cycle.),

e. edge detecting valid instructions occurring after the complex instruction during at least one of the first clock cycle and the second clock cycle (The system of Panwar is clocked. At each active clock cycle edge valid instructions are detected and marked as such in element 710 of Figure 7.); and

f. executing the valid instructions occurring after the complex instruction during a third clock cycle (column 10, lines 4-22).

21. Referring to claim 18, Panwar has taught an apparatus for calculating the number of valid instructions within a microprocessor (Figure 7, element 710 stores the calculated number of valid instructions within the microprocessor.), comprising:

a. a mechanism for fetching a bundle of instructions (Figure 2, element 202),

b. a advancing mechanism for advancing instructions along a microprocessor pipeline (column 3, line 15-column 4, line 2), and

c. an edge detection element for detecting valid instructions within the bundle (The system of Panwar is clocked. At each active clock cycle edge valid instructions are detected and marked as such in element 710 of Figure 7.).

22. Referring to claim 19, Panwar has taught an apparatus according to claim 18, as described above, and further comprising a shifting mechanism for shifting at least one instruction based at least in part on the number of valid instructions in the bundle (Figures 5-9, The number of valid instructions determines which instructions are shifted and to where they are shifted.).

23. Referring to claim 20, Panwar has taught an apparatus according to claim 18, as described above, and further comprising a compression mechanism, wherein said compression mechanism compressed a bundle of instructions for a monotonic instruction bundle (Figure 5, element 500B).

24. Referring to claim 21, Panwar has taught the apparatus according to claim 18, as described above, and further comprising a compression mechanism, wherein said compression mechanism compressed a bundle of instructions based at least in part on the number of valid instructions in the bundle (Figures 5-9, The number of valid instructions determines which

instructions are shifted and to where they are shifted such that each sub-bundle is a compressed version of the main bundle, element 203.).

25. Referring to claim 22, Panwar has taught the mechanism, apparatus according to claim 18, as described above, and further comprising a bundling mechanism, wherein said bundling mechanism bundles instructions occurring prior to a complex instruction (column 10, lines 4-22, Figure 5-9, instructions A, B, and C are bundled in sub-bundle 500A.).

26. Referring to claim 23, Panwar has taught an apparatus in accordance with claim 18, as described above, and further comprising an execution mechanism, wherein said execution mechanism executes instructions occurring prior to a complex instruction during a first clock cycle (column 10, lines 4-22).

27. Referring to claim 24, Panwar has taught an apparatus in accordance with claim 18, further comprising an execution mechanism, wherein said execution mechanism executes a complex instruction during a second clock cycle (column 10, lines 4-22).

Response to Arguments

28. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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